the appended claims encompass any such modifications or embodiments.

WE CLAIM:

1. A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer over said silicon substrate;

forming a second dielectric layer over said first dielectric layer wherein the dielectric constant of the second dielectric layer is less that 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN),

titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

forming a trench in said second dielectric; and

filling said trench with a conducting material.

2. The method of claim 1 wherein said second dielectric layer is OSG.

3. The method of claim 1 wherein said conducting material is copper.

4. The method of claim 1 wherein the material used to form the first hardmask layer is selected from the group consisting of silicon carbide and silicon nitride.

5. A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer over said silicon substrate;

forming a second dielectric layer over said first dielectric layer wherein the dielectric constant of the second dielectric layer is less that 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

etching a first opening in said second hardmask layer of a first width;

forming a first trench of a second width in said second dielectric layer wherein said second width is less than said first width;

etching a second opening in said first hardmask layer of a first width;

forming a second trench of a first width in said second dielectric layer wherein said second trench is positioned over said first trench; and

filling said first and second trench with a conducting material.

6. The method of claim 5 wherein said second dielectric layer is OSG.

7. The method of claim 5 wherein said conducting material is copper.

8. The method of claim 5 wherein said first hardmask is a material selected from the group consisting of silicon nitride and silicon carbide.

9. A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first etch stop layer over said silicon substrate;

forming a first dielectric layer over said first etch stop layer wherein the dielectric constant of the first dielectric layer is less than 3.0;

forming a second etch stop layer over said first dielectric layer;

forming a second dielectric layer over said first etch stop layer wherein the dielectric constant of the second dielectric layer is less that 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said second first hardmask layer wherein said second hardmask layer comprises

a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

etching a first opening in said second hardmask layer of a first width;

forming a first trench of a second width in said second dielectric layer wherein said second width is less than said first width;

etching a second opening in said first hardmask layer of a first width;

forming a second trench of a first width in said second dielectric layer wherein said second trench is positioned over said first trench;

simultaneously etching said second trench to a depth of said second etch stop layer and said first trench to a depth of said first etch stop layer; and

filling said first and second trench with a conducting material.

10. The method of claim 9 wherein said first dielectric layer is OSG.

11. The method of claim 9 wherein said second dielectric layer is OSG.

12. The method of claim 9 wherein said conducting material is copper.

13. The method of claim 9 wherein said first hardmask is a material selected from the group consisting of silicon nitride and silicon carbide.